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VLSI Implementation of Ternary Gates MultiValue System

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Abstract
CMOS logic is taken into account for implementation of solely binary logic, because the circuit complexness is increasing, the interconnection in binary occupies massive space on VLSI chip & so, degrading the performance. MVL (Multi valued logic) is taken into account as resolution to the current issue. A Ternary logic or three-valued logic is taken into account as best base of many MVL systems.
The planned GATES area unit styled & simulated with the assistance of Tanner EDA tool and layout design victimization VLSI CMOS technology. Planned system: In style of digital systems, the electrical converter, NOR gate & NAND gates area unit thought-about to be building blocks. The most objective is to reduce the facility consumption & propagation delay time thereby reducing the quantity of electronic transistor.
In the planned styles, the smaller single provide voltage & MOSFETs with smaller threshold voltage area unit used. 3 logic levels area unit drawn by states zero, 1, a pair of with potential (0v), (0.5v), & +Vcc (+1v) severally. Within the planned styles, these output transmission gates/pull up transistors area unit eliminated from inverters, thereby reducing the part count.
Use of single power provide to implement ternary logic gates has result in important reduction in overall power dissipation & rising the transition time Considering the varied benefits of the MVL, the acceptable style of MVL logic gates is vital so it'll result in the more development and its application in this area.

Keywords: VLSI, Multi Valued Logic, Ternary, Logic Gates

Introduction
MultipleValued logic has been the object of much research over the last 30 years. Since 1971 there has been an annual symposium devoted exclusively to the object [1]. In addition, a large number of technical papers have appeared elsewhere together with number of survey articles. Much of the older work was purely theoretical nature concerned with the functional completeness of sets of operator, functional minimization and similar problems from the switching theory and logic design. Work on hardware implementation of multiple value devices has been more recent. The application of Multi Valued Logic spans the full range of areas from application to VLSI technology and design techniques [2][3][4][5].
Recent technical work has shown some advantages of using multi-valued logic where the natural question is whether there exists a practical radix other than 2 that would produce circuits with greater saving in components, without loss of speed. Alexander (1964) showed that the most efficient radix for
implementation of switching systems is the natural base (e=2.71828). From which it appears that the closest natural integral radix should be 3 rather than 2 [6].
Ternary gives meaning of a transmission and 3- valued switching. Three-valued or ternary, logic offers several important advantages over binary logic in design of digital systems. For example, more information can be transmitted over a given set of lines or stored for a given length, the complexity of interconnections can be reduced, reduction in chip area can be achieved, and more easy error detection and error correction codes can be employed. Furthermore, serial and some serial-parallel arithmetic operations can be carried out at higher speeds. Many of these advantages have direct bearing on the implementation of digital

systems, and as a result, realizations of basic ternary gates have been proposed. These have been shown to be suitable for the design of "ternary processors" and for various other applications [7] [8] [9].

It has been reported that realization of combinational and sequential logic functions is possible in a ternary logic element. In addition, they have proposed an implementation of the T-gate using bi-polar transistors, and considered for application to the synthesis of combinational as well as logical circuits. Recently, researchers have proposed an alternative implementation of the T-gate MOS technology. The synthesis of suitable combinational circuit requires $(3^N–1)/2$ T-gates where N= number of inputs. Ternary logic family comprises of set of inverters, NOR gate and NAND gate. These circuits are used to design ternary memory elements and some basic ternary arithmetic circuits like half adder and full adders, and one-ternary multiplier. The circuits thus obtained are then used to synthesize a shift register, an N-bit adder, and an N-bit multiplier.

An objective of present research work is to design and simulation of CMOS ternary logic gates (T-Gates) to implement basic ternary operations like AND, OR, NAND, NOR, NOT etc.

Ternary Logic Preliminaries

Among the MVLs, ternary logic is distinctive because of its simpler circuit realization and a well-established theoretical basis [11]. Many ternary logic models exist in the literature, but they generally involve high power consumption even in static state [12]. Customized technological processes [4] or multi-threshold devices [13], Current-mode MVL techniques also exist [10], but they are not feasible for present high performance applications as high-speed performance and low– power dissipation can be obtained using the CMOS technology. In voltage mode operation of circuit the three distinct logic levels are defined in terms of voltage where as in current mode operation, states are integral multiple of reference current. Figure 1 shows ternary levels in terms of voltage as low (V_L), intermediate (V_I) & high (V_H). Low voltage level corresponds to logical state 0; intermediate to logic state 1 & high to logic state 2 respectively. The logical symbolism assumed is given in table 1. To implement ternary system basic Boolean operations that are necessary are, ternary inverter, Ternary OR/NOR (T-OR/T/NOR), Ternary AND/NAND (T-AND/T-NAND) and Ternary EX-OR/NOR (T-EX-OR/T-EX-NOR). These operations are carried out by ternary logic gates (T-gates). Recent articles show that there is still an ongoing improvement in the implementation of T-gates [14] [15]. However, basic T-gate circuit implementations are considered in the present work using latest switching circuit devices. *Haider et al.* [16] introduced a new set of ternary neural networks to realize a novel TALU and used *MATLAB Simulink* as a simulation tool to demonstrate the feasibility, functionality and the correctness of the neural network design. *Dhande et al.* [17] designed and implemented 2 bit ternary ALU slice using CMOS ternary logic gates. However, in most of the studies, there still remains out-sized scope to evaluate the reductions techniques in digital designing, especially for the ternary circuits.

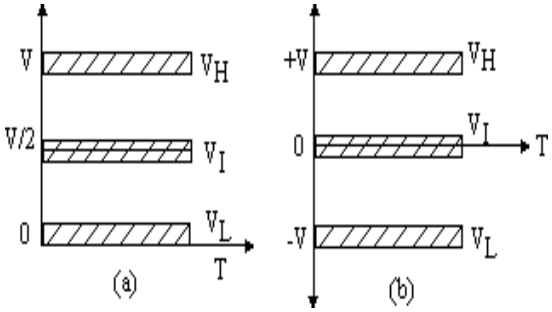


Fig 1: logic levels in Ternary system (a) when supply voltage is o to +v volt
(b) When supply voltage is –v to +v volt

Table I: Logical Symbol for Ternary System.

(a) Supply voltage 0 to +V

Voltage Level	Logic Level
V	2
V/2	1
0	0

(a)

(b) Supply voltage –V to +V

Voltage Level	Logic Level
+V	2
0	1
-V	0

(b)

This may further give additional circuit reduction, thereby reducing the delays and the complexity in VLSI designing. In a VLSI circuit, approximately 70 percent of the area is devoted to interconnection, 20 percent to insulation, and 10 percent to devices [18]. Ternary (three valued) or trivalent logic is an example of multi-valued logic in which the states are 0, 1 and 2

[19] which serves as a potential and a promising solution in advancements of technology

A. Ternary Inverter

The Yoeli-Rosinfeld algebra [11] defines three basic ternary elements, the STI (simple ternary inverter) PTI (positive ternary inverter) & NTI (Negative ternary inverter) such that,

$$STI = X \quad = 2 - X$$

$$\text{—} \quad \vartheta\, i \rightarrow X \sigma\, i \qquad \ldots\ldots (2.1)$$

$$PTI \ , NTI \quad = X^i \quad = \begin{cases} \\ \square\ 2 - i \rightarrow X = i \end{cases}$$

Where 'i' take the value of '2' for PTI & '0' for NTI inverter. Basic switching elements in the implementation of those inverters are transistors, MOSFET & RTDs. Because of low power consumption, less propagation time, high low power consumption, less propagation time, high fan in\out, high voltage swing and operation in GHz domain, circuits based on MOSFET of RTDs are more popular,[14][15]. Figure 2 shows MOS based three inverters namely STI, PTI & NTI. Truth table for the same is given in Table 2. Symbol for the ternary inverter is shown in figure 3.

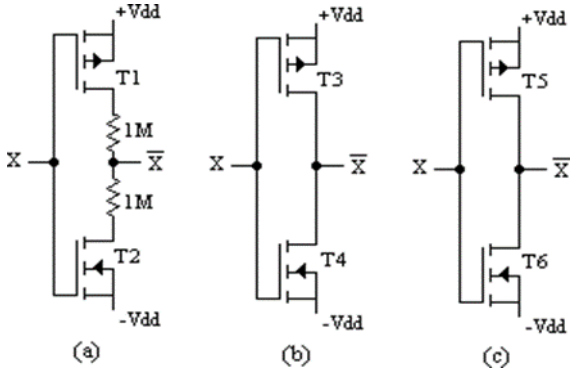


Fig 2: CMOS implementation of T-Inverter (a) STI (b) PTI (c) (NTI).

Table II: Truth Table for Inverter.

Input X	Output		
	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

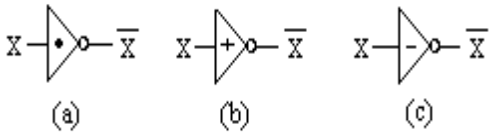


Fig 3: Symbols for Inverters (a) STI (b) PTI (c) NTI

B. Ternary OR /NOR circuit

Ternary OR is a circuit that have X_1---X_n as input & Y_o as output such that

$$T-OR \quad = X^{1} + X^{2} + \ldots\ldots + X^{n} = Max\,[X_1, X_2, \ldots X_n] \quad \ldots\ldots (2.2)$$

Ternary NOR has an output that is a compliment of OR function i.e.

$$T-NOR \quad = \overline{X^{1} + X^{2} + \square + X^{n}} = \overline{Max\,[X_1, X_2 \ldots X_n]} \ldots (2.3)$$

The sign + indicates logical ternary OR operation. Inverter is a basic circuit that is used for implementing T-OR/NOR functions [11]. Depending upon the type of inverter used, the logic functions T-OR/NOR can be a) simple ternary OR/NOR [ST-OR/NOR], b) Positive ternary OR/NOR [PT-OR/NOR], c) Negative ternary OR/NOR [NT-OR/NOR]. Fig 4 shows Symbols for T-OR/NOR logic gates.

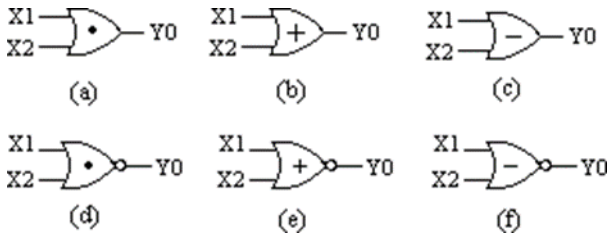


Fig 4: Symbols for T-OR/NOR logic gates (a) ST-OR (b) PT-OR (c) NT- OR (d) ST-NOR (e) PT-NOR (f) NT-NOR.

III. Design and Simulation of the Ternary Gates.

Tanner Tool is reported to be potential EDA software for designing and verification of various VLSI circuits. The T-gates designed in this paper are implemented using Tanner tool, version 13.02 on machine of core 2 duo processor, 2 GHz,
1 GB RAM. S-Edit, L-Edit, T-Spice and W-Edit are the prominent subsets of the tanner tool that are used to derive the various device parameters and further verify the functionality of the gates. The gates in the original binary logic diagram of the circuit are conceptually transformed into corresponding ternary ones using the injected voltage method [20].

This paper uses three voltage levels (0 V, 2.5 V, 5V) to represent three ternary logic levels (0, 1, and 2). Figure 6(a) depicts a simple ternary inverter (STI) which is composed of nMOS, pMOS and a resistor 'R'. Vdd (voltage source 1) is 5V and auxiliary power supply (voltage source 2) is 2.5 V. The absolute value of thresholds (VTp, VTn) is raised for the MOS transistors, wherein VTp = -3.75V and VTn = 3.75 V. This is accomplished by changing W/L (Width / Length) ratio of the MOS transistors and the corresponding multiplier factor 'M'. When input level is 2.5 V, both pMOS and nMOS transistors and the output nodes will be 2.5V due to the connected auxiliary supply. Obviously, on the resistor there will be a current of 2.5 V/R drawing out of the auxiliary supply if the node value is 0 V, and a current of 2.5 V/R injecting into the auxiliary supply if the node value is 5 V. The layout is designed using L-edit as depicted in figure 6(b). Both, the layout and the schematic of the STI are independently verified using T-spice and W edit. Figure 6 (c) illustrates the simulation results of STI, verified for all the combinations of the input. Other universal gates, T-NAND and T-NOR have also been implemented in a similar fashion. Figure 7 indicates the schematic, layout and simulation results of the T-NAND. Encouraging results are obtained for T-NOR gate as well.

Additional performance analysis of the designed basic gates has been carried out in terms of calculating the rise time and fall time during all the logic transitions (0-1, 1-2 and 0-2). The average dissipated power across the resistor and the MOS transistors is also obtained. Table 3 and Table 4 summarizes the achieved results.

Table III: Timing Parameters of the Ternary Gates.

Parameter	Logic level	TNOT	TNAND	TNOR
Rise Time	0 to 1	0.74 ns	2.32 ns	2.02 ns
Rise Time	1 to 2	0.74 ns	1.47 ns	1.38 ns
Rise Time	0 to 2	1.69 ns	0.50 us	0.50 us
Fall Time	2 to 0	0.50 us	2.50 us	1.62 ns
Fall Time	2 to 1	1.58 ns	2.10 ns	0.71 ns
Fall Time	1 to 0	1.43 ns	0.73 ns	0.71 ns

Table IV: Performance Parameters of the Ternary Gates

Average Power	TNOT	TNAND	TNOR
MOS Transistors	0.289 uw	1.216 uw	75.62 uw
Resistor	0.378 mw	3.103 uw	98.77 uw

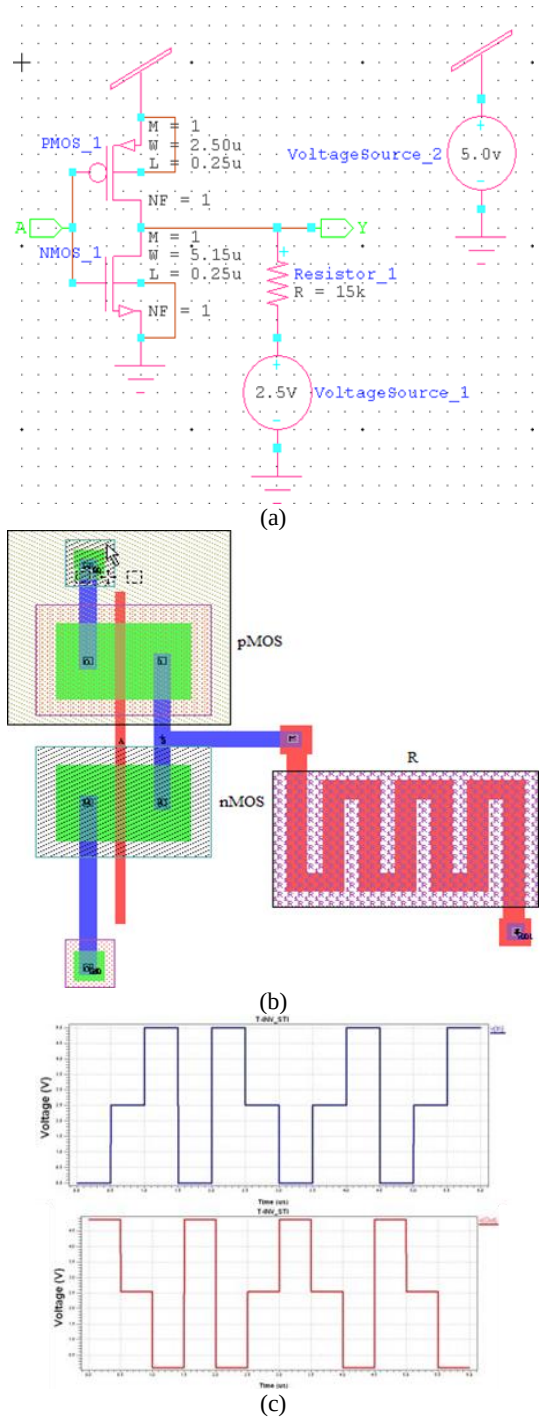
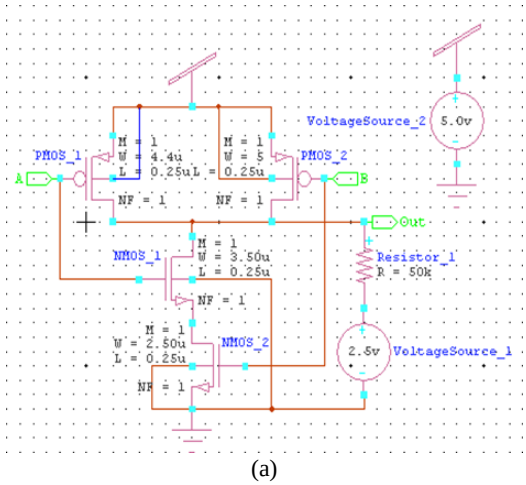


Fig 6: Results of TNOT gate (STI gate) (a) schematic (b) layout (c) simulation results.



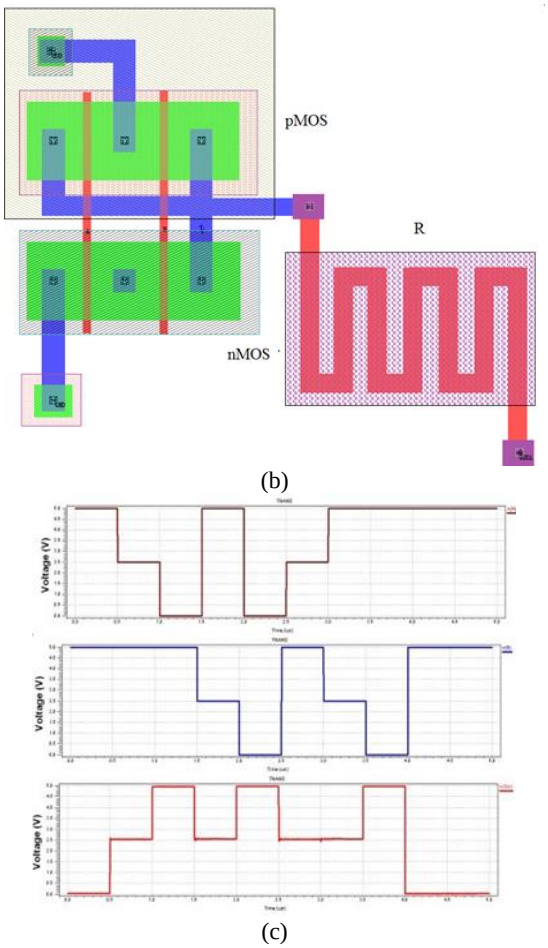


Fig 7: Results of TNAND gate (a) schematic (b) layout (c) Simulation results.

Conclusion

Tanner tool has been exploited to design and implement CMOS Ternary logic gates. The layouts and the simulation results along with performance analysis is also been presented in the paper. The Voltage values for the ternary logic levels were tested for STI, ST-NAND and ST-NOR. The same procedure can be easily extended to design positive and negative ternary logic gates by adjusting the auxiliary supply voltage at 0V and -2.5 V respectively.

The choice of the resistance value greatly affects the voltage levels at the output of the T-gates. This paper examines the performance of designed T gates to estimate the suitable value of resistance. Encouraging results are obtained with R= 15 K in case of STI whereas ST-NAND and ST-NOR give best results with R=50 K. The value of R thus varies with the design. W/L ratio is another important parameter that has a significant impact on the design of the T-gates. This ratio affects the threshold voltage of the MOS transistors. In the proposed design, W/L ratio is suitably maintained to achieve desired voltage values at the output.

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